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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/848,846
Filing Date: May 03, 2001
Appellant(s): TRAN, LUAN C.

Deepak Malhotra
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/23/05 appealing from the Office action mailed 3/23/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

No evidence is relied upon by the examiner in the rejection of the claims under appeal.

It is assumed that the Appellant meant to include both Evidence and Related Proceedings appendixes with a statement of "NONE.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 11-12 and 14 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Lowrey et al ('504).

In reference to claim 11, Lowrey teaches a semiconductor processing method comprising:

a masking step providing a common mask; and

an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least two of the devices two different respective threshold voltages, wherein the common masking step comprises masking only portions of some of the devices which receive the halo implant, said portions comprising portions of peripheral circuitry devices (Fig.6 and Col.6, lines: 60-65; see also Col.2, lines: 1-20).

In reference to claim 12, Lowrey teaches a semiconductor processing method comprising:

a masking step providing a common mask (Col.2, lines: 1-20); and

an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least two of the devices two different respective threshold voltages, wherein the common masking step comprises masking only portions of some of the devices which receive the halo implant , said devices which receive the halo implant comprise NMOS field effect transistors; and said portions comprise portions of peripheral circuitry devices (Col.2, lines: 1-20 and Col.6, lines: 60-65 and Fig.6).

In reference to claim 14, Lowrey teaches a semiconductor processing method comprising: a masking step providing a common mask; and an implant step carried out through the common mask, comprising conducting a halo implant of devices formed over a substrate comprising memory circuitry and peripheral circuitry sufficient to impart to at least two of the devices two different respective threshold voltages, wherein the common masking step comprises masking only portions of some of the devices which receive the halo implant', said devices which receive the halo implant comprise PMOS field effect transistors', and said portions comprise portions of peripheral circuitry devices (Col.2, lines: 1-20 and Fig.6 and Col.6, lines: 60-65).

However with respect claims 11-12 and 14, Lowrey fails to teach three different transistors having three different threshold voltages. However, the courts have held that mere duplication of parts has no patentable significance unless a new or unexpected result is produced see In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960). Therefore Appellant's claim language is considered to be an obvious variation of Lowrey's teachings.

(10) Response to Argument

The Appellant argues that the Examiner has not compared the facts of Harza to the facts of the current application. The Appellant also argues that Lowrey fails to suggest to one of ordinary skill in the art the desirability of three different transistors having three different threshold voltages. (See pages 5-6, Appellant's Appeal Brief).

The MPEP 2144.04 VI (B) states, that "In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960) (Claims at issue were directed to a water-tight masonry structure wherein a water seal of flexible material fills the joints which form between adjacent pours of concrete. The claimed water seal has a "web" which lies ** in the joint, and a plurality of "ribs" ** >projecting outwardly from each side of the web into one of the adjacent concrete slabs. <The prior art disclosed a flexible water stop for preventing passage of water between masses of concrete in the shape of a plus sign (+). Although the reference did not disclose a plurality of ribs, the court held that mere duplication of parts has no patentable significance unless a new and unexpected result is produced.)."

The Lowrey reference teaches multiple transistors for a reverse poly DRAM where at least two transistors have their threshold voltages manipulated- the peripheral transistor has a reduced threshold voltage and the access transistor has a higher threshold voltage (Col.2, lines: 1-17). Similar to the ribs of Hazra, the prior art reference fails to explicitly teach forming a third transistor with a third threshold voltage, however it would be obvious to have a third transistor formed with a third threshold voltage because DRAM devices may include hundreds of transistors, such as read-out transistors which would have a third threshold voltage, different from the peripheral and access transistors. As the Courts held in Hazra, the mere duplication of modifying a third transistors' threshold voltage has no patentable significance. It is merely the repetition of having a third transistor on a memory device which has a third threshold voltage.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer. **It is assumed that the Appellant meant to include both Evidence and Related Proceedings appendixes with a statement of "NONE.**

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Laura Schillinger, Primary Examiner

Conferees:

Carl W. Whitehead, Jr., SPE

Ricky Mack, SPE